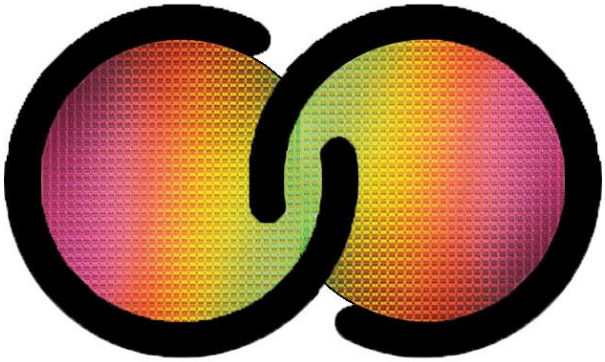
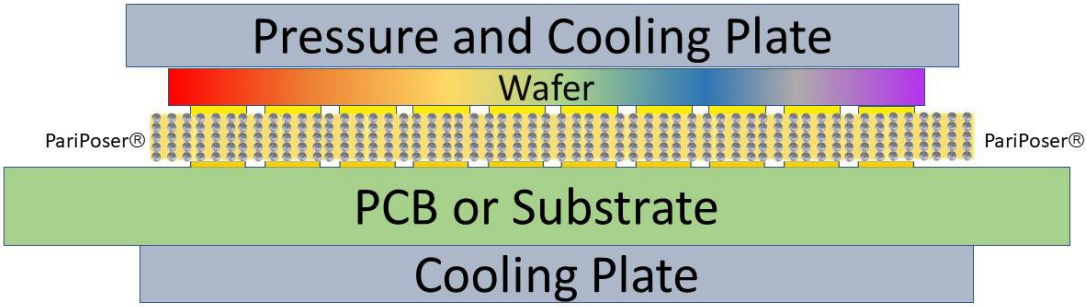
Wafer Connectors

Rev: Oct 2, 2019



What is a wafer Connector ?

A wafer connector is in interconnect directly between an unpackaged Integrated Circuit (IC) and some type of a platform (PCB or ceramic substrate). The platform typically delivers power, ground, and signal lines to the IC. The application might be either for testing, or for final packaging.



A wafer connector concept using the PariPoser® anisotropic elastomer

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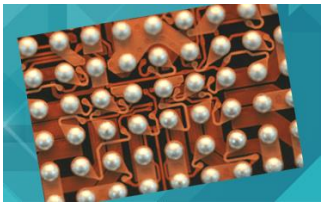
Why use a wafer connector ?

1) Wafers can be made bigger, and can be interconnected more efficiently.

2) The packaging density can improve.

3) Power and ground distribution to the wafer are better.

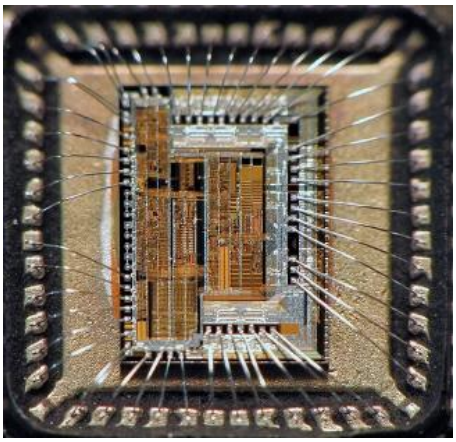
4) Wafers can be interconnected in a grid array pattern.



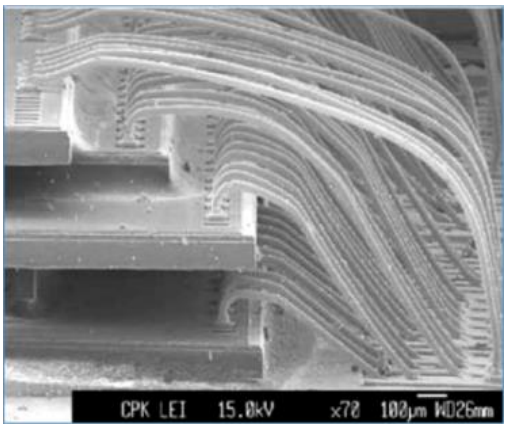
5) Wafers can the tested before final packaging.

What is used now for wafer interconnects ?

75% of IC packages use wire bonding from the IC pads to platform pads (lead frames, substrate, etc.).



Single die



Multiple dies

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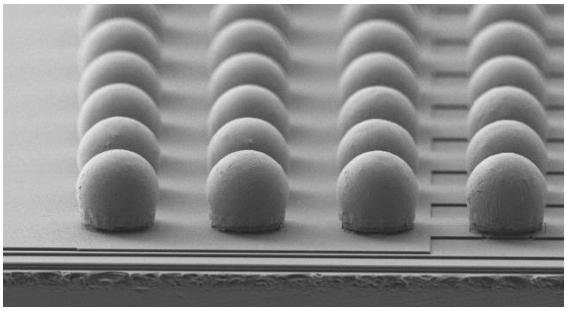
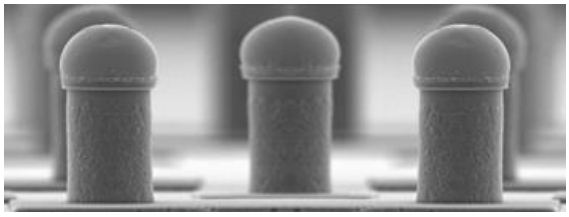
Sometimes, solder bumps are placed on the I/O pads of dies and then the die is flipped over and soldered to the platform.



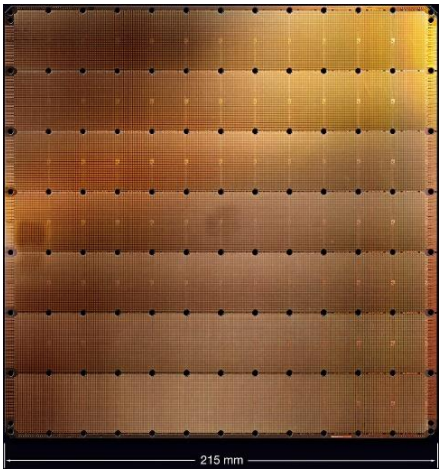
A new technique is to additively plate copper pillars on the I/O pads of the IC (with a little dab of solder on the top). The die is then flipped over and soldered to the platform.



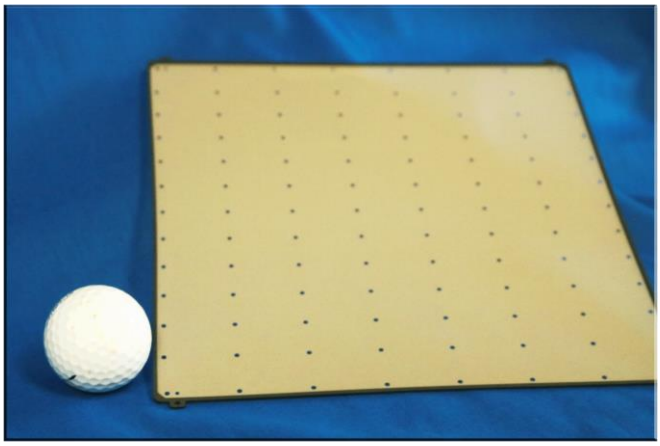
Is a wafer connector a real thing ?

It's a new thing. But, it's also a real thing.

The 219mm x 219mm (8.62" x 8.62") wafer connector shown below is used by Cerebras for their mammoth ICs. (Ref: www.cerebras.net) It's made with a continuous sheet of PariPoser® material mounted on a thin aluminum frame. It is used in their delivered product.



Cerebras 215mm x 215mm wafer



The Paricon wafer connector

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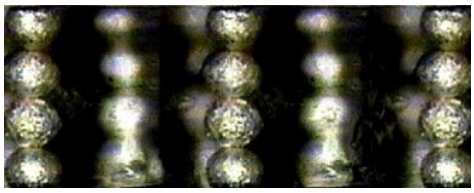
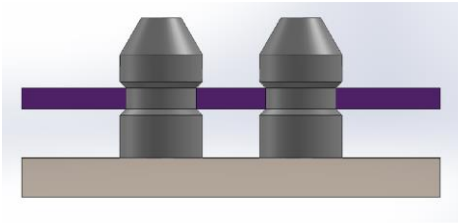
What Paricon products are used in making a wafer connector ?

PariPoser® material uses conductive columns of nickel nanoparticles in a dense and economical array to connect a wafer to a substrate



PariProbes® can be added to the PariPoser® material to handle unusual target shapes.



Spring pins can be used if the I/O pad pitch is big enough.

A brief recap about Paricon's conductive elastomers.

Paricon's PariPoser® material is an anisotropic conductive elastomer with magnetically aligned columns of nickel nanoparticles. The material is made in large sheets with the columns formed along the many magnetic flux lines of the production magnet. After curing, the columns stay in alignment.

When compressed, the columns conduct current vertically, but not horizontally.

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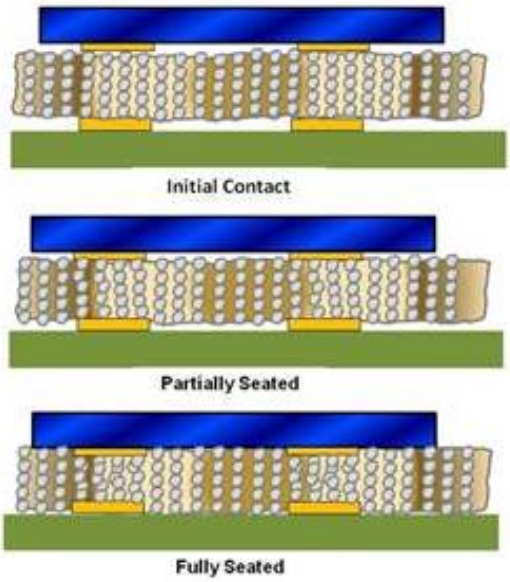
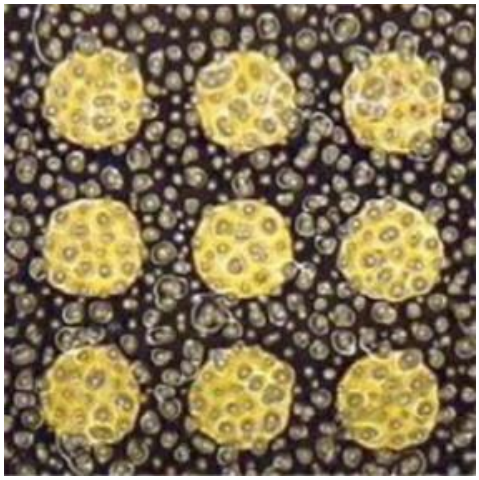


Prior to compression, the nickel nanoparticles at the end of the columns stick out a bit from the silicone. When compressed, they push against each other and form a low CRES signal path from the device pad to the substrate pad.

The interstitial area between pads are filled with the elastomer that has been squeezed away from the contacts.



There are typically 6-10 nickel nanoparticle columns for each pad. (And, many columns that are not used.) The locations of the columns are based on the magnetic flux lines of the production magnet.

A full explanation of the PariPoser® technology is found on the Paricon web site.

How about a PariPoser® wafer connector ?

The I/O pads on the wafer are the first consideration. They need to be designed for a direct contact with the elastomer instead of a bonding wire or a solder ball. The I/O pad pitch can be in the 0.2mm to 0.4mm range, and the pads typically have a diameter equal to 60% of the pitch. They also need to be flat with a small elevation of about 15 µm above the wafer surface.

The shape of substrate pads should match the shape of the IC pads. The substrate contact pads are typically elevated by a similar value, and the interstitial areas between the pads needs to be free of solder mask or other items that might interfere with the material.

The wafer needs to be pushed against the connector with a **force** of about 5-10 grams per I/O pad (when the layout of the pads are in a grid based on Paricon's design rules). Overall, that's a **pressure** of 57 grams/mm^2 (70 psi) over the entire elastomer because the elastomer is pushed down on the I/O pads and the interstitial areas at the same time. Typical spring or cantilever contact mechanisms require a force of 30 – 50 grams per I/O pad.

The pusher can also act as a cooling device.

The substrate needs to be flat – even with the wafer being pushed down on it. If the substrate is thin or subject to bending, it will need a backer plate on the back side of the substrate. This too can be part of the cooling system for the connector assembly.

Due to the low metal content of the PariPoser® material, the connector will not take a set, and will be quite durable for hundreds of thousands of cycles and years of engagement.

The thermal management of the connector assembly needs careful attention because the Coefficient of Thermal Expansion (CTE) of the individual elements varies a lot.

Material	**CTE**	
Silicon	2.6	
Silicone	6-8	The primary material in a PariPoser®
PCBs	14-17	
Cored PCBs	9-12	Low CTE material is layered in the core
Ceramics	3-6	Sometimes used in a substrate
Kapton	20	
Metals	10-30	Brass, Aluminum, Nickel, etc.
Low CTE metals	5-10	Kovar, Alloy 42

Typically, the material CTEs have to match, or otherwise there needs to be an aggressive cooling apparatus engaged.

The connector materials are individually rated up to 150°C. The temperature rating of the connector assembly will depend on the selection of the other materials, the proximity of conductors, and the power demands that are present during use.

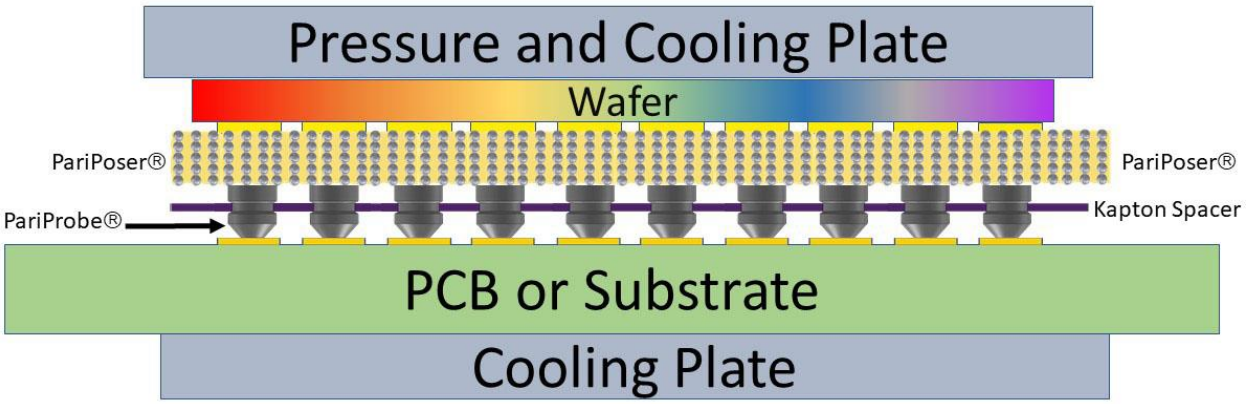
How about a PariProbe® wafer connector ?

A PariProbe® layer can be used with the PariPoser® elastomer material.

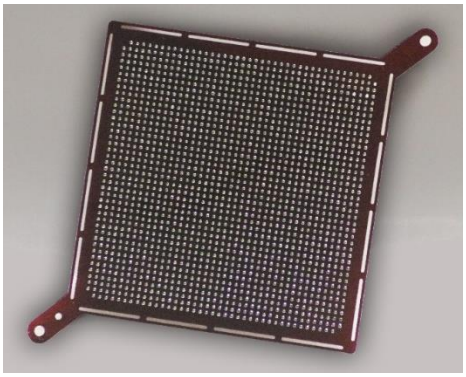
The additional benefits of including this layer are:

The shape of the PariProbe® contact allows engagement with odd-shaped pads.

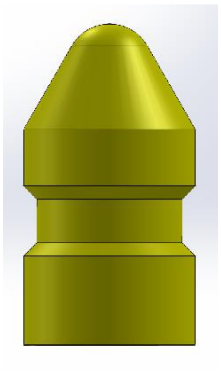
It's possible to use the PariProbe® layer to manage CTE differences in the connector system. (lateral motion, air flow, etc.)



A wafer connector concept using a PariProbe® layer



A 45mm x 45mm array of PariProbes®



A typical PariProbe®

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Additional information about PariProbe® interconnects is found in the Technology Section of the Paricon web page (PariProbe® Primer).

How about spring pin wafer connectors ?

If the wafer I/O pitch is > 0.2mm, then spring pins are a feasible alternative.

A wafer connector concept using traditional spring pins